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09/813,087	03/19/2001	Frank R. Bryant	10004055-1	1395

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/813,087	Applicant(s) BRYANT ET AL.
	Examin r Monica Lewis	Art Unit 2822

-- Th MAILING DATE of this communication appears on the cover sh t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *29-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *11 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed July 10, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5-9, 11, 12, 15-19, 21-24, 27 and 28 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Burke et al. (U.S. Patent No. 6,102,528) and Matta (U.S. Patent No. 6,183,067).

In regards to claim 1, Hess et al. ("Hess") discloses the following:

a) a substrate (70) (For Example: See Figure 11);

b) a set of transistors (74) formed in the substrate (For Example: See Figure 11 and Column 5 Lines 32 and 33); and

c) an ejection element (109) coupled to at least one of the set of transistor (For Example: See Figure 11).

In regards to claim 1, Hess fails to disclose the following:

a) a set of transistors wherein the gate of each of the set of transistor forms at least one closed loop.

However, Burke et al. ("Burke") discloses transistors wherein the gate forms a closed loop (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include transistors wherein the gate forms a closed loop as disclosed in Matta because it aids in eliminating punch through (For Example: See Column 1 Lines 1-67 and Column 2 Lines 1-62).

Additionally, since Hess and Burke are both from the same field of endeavor, the purpose disclosed by Burke would have been recognized in the pertinent art of Hess.

b) an ejection element is disposed over the substrate without an intervening field oxide layer.

However, Matta discloses an ejection element (18) disposed over the substrate (10) (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include an ejection element is disposed over the substrate without an intervening field oxide layer as disclosed in Matta because it aids in improving the manner in which ink is projected which ultimately improves the print quality (For Example: See Column 1 Lines 12-55).

Additionally, since Hess and Matta are both from the same field of endeavor, the purpose disclosed by Matta would have been recognized in the pertinent art of Hess.

In regards to claims 2 and 12, Hess discloses the following:

a) a dielectric layer disposed between the ejection element and the substrate having a thickness greater than 2,000 Angstroms (For Example: See Column 5 Lines 22-24).

In regards to claims 5 and 15, Hess discloses the following:

a) each of the set of transistors has a bulk that is not directly connected to the substrate (For Example: See Figure 11).

In regards to claims 6 and 16, Hess fails to disclose the following:

a) the set of transistors is formed with without an active mask definition.

However, the limitation of "active mask definition" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claims 7 and 17, Hess discloses the following:

a) the set of transistors has a gate oxide formed with a layer of silicon dioxide (72) and a layer of silicon nitride (122) (For Example: See Figure 11).

In regards to claims 8 and 18, Hess discloses the following:

a) an orifice layer (140) defining a nozzle fluidically coupled to the ejection element and wherein the nozzle is further fluidically coupled to a fluid channel to deliver fluid to the ejection element (For Example: See Column 8 Lines 26-44).

In regards to claims 9 and 19, Hess discloses the following:

a) a body having a fluid reservoir fluidically coupled to the fluid channel of the printhead (For Example: See Figure 10); and

b) a pressure regulator for maintaining a negative pressure relative to the ambient air pressure to prevent the fluid within the printhead from drooling out of the nozzle without activation of the ejection element (For Example: See Column 8 Lines 39-41).

In regards to claim 11, Hess discloses the following:

a) a substrate (For Example: See Figure 11);

b) a set of transistors formed in the substrate (For Example: See Figure 11 and Column 5 Lines 32 and 33); and

c) an ejection element coupled to the transistor (For Example: See Figure 11).

In regards to claim 11, Hess fails to disclose the following:

a) the transistors are formed with at least one closed loop.

However, Burke discloses transistors wherein the gate forms a closed loop (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include transistors wherein the gate forms a closed loop as disclosed in Matta because it aids in eliminating punch through (For Example: See Column 1 Lines 1-67 and Column 2 Lines 1-62).

Additionally, since Hess and Burke are both from the same field of endeavor, the purpose disclosed by Burke would have been recognized in the pertinent art of Hess.

b) an ejection element is disposed over the substrate without an intervening field oxide layer.

However, Matta discloses an ejection element disposed over the substrate (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include an ejection element

is disposed over the substrate without an intervening field oxide layer as disclosed in Matta because it aids in improving the manner in which ink is projected which ultimately improves the print quality (For Example: See Column 1 Lines 12-55).

Additionally, since Hess and Matta are both from the same field of endeavor, the purpose disclosed by Matta would have been recognized in the pertinent art of Hess.

In regards to claim 21, Hess discloses the following:

a) a substrate (For Example: See Figure 11);

b) each transistor positioned on the substrate, the transistor comprising a source region (76), a drain region (79), and a gate (78) positioned between the source region and the drain region (For Example: See Figure 11 and Column 5 Lines 32 and 33);

c) a layer of silicon dioxide not of field oxide disposed over the substrate, and a layer of polycrystalline silicon (80) directly on the layer of silicon dioxide (For Example: See Figure 11);

d) a layer of dielectric material covering the substrate having a plurality of openings there through, the openings providing access the source region, the drain region, and the gate of the transistor (For Example: See Column 5 Lines 22-24);

e) a layer of electrically resistive material positioned on the layer of dielectric material and in direct electrical contact with the source region, the drain region, and the gate through the openings (For Example: See Column 6 Lines 5 and 6);

f) a layer of conductive material (100) affixed to a portion of the layer of electrically resistive material in order to form a multi-layer structure, the layer of electrically resistive material having at least one uncovered section capable of functioning as an ejection element, the layer of electrically resistive material being covered with the layer of conductive material at the source region, the drain region and the gate of the transistor (For Example: See Figure 11);

g) a portion of protective material positioned on the ejection element (For Example: See Figure 11); and

h) an orifice layer having at least one nozzle, the orifice layer secured to the portion of protective material having a section thereof removed directly beneath the nozzle in order to form a fluid well in order to impart energy from the ejection element (For Example: See Figure 11).

In regards to claim 21, Hess fails to disclose the following:

a) the gate forming a closed loop.

However, Burke discloses transistors wherein the gate forms a closed loop (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include transistors wherein the gate forms a closed loop as disclosed in Matta because it aids in eliminating punch through (For Example: See Column 1 Lines 1-67 and Column 2 Lines 1-62).

Additionally, since Hess and Burke are both from the same field of endeavor, the purpose disclosed by Burke would have been recognized in the pertinent art of Hess.

In regards to claim 22, Hess discloses the following:

a) the layer of electrically resistive material is comprised of a mixture of tantalum and aluminum (For Example: See Column 6 Lines 5 and 6).

In regards to claim 23, Hess discloses the following:

a) the layer of electrically resistive material is comprised of polycrystalline silicon (For Example: See Column 6 Lines 17 and 18).

In regards to claim 24, Hess discloses the following:

a) the layer of conductive material comprises a metal selected from the group consisting of aluminum, copper, and gold (For Example: See Column 6 Lines 50-52).

In regards to claim 27, Hess discloses the following:

a) the transistor has a gate oxide a layer of silicon nitride disposed between the gate and substrate (For Example: See Figure 11).

In regards to claim 28, Hess discloses the following:

a) a first passivation layer positioned on the ejection element, the first passivation layer being comprised of silicon nitride (For Example: See Column 7 Lines 33 and 34 and Figure 11);

b) a second passivation layer positioned on the first passivation layer, the second passivation layer being comprised of silicon carbide (For Example: See Column 7 Lines 49 and 50 and Figure 11);

c) a cavitation layer positioned on the second passivation layer, the cavitation layer being comprised of a metal selected from the group consisting of tantalum, tungsten, and molybdenum (For Example: See Column 7 Lines 66 and 67); and

d) a fluid barrier layer (130) positioned on the cavitation layer, the fluid barrier layer being comprised of plastic, the orifice layer being secured to the fluid barrier layer (For Example: See Column 8 Lines 7 and 8).

5. Claims 3, 13 and 25 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Burke et al. (U.S. Patent No. 6,102,528), Matta (U.S. Patent No. 6,183,067) and Hess (U.S. Patent No. 4,719,477).

In regards to claims 3, 13 and 25, Hess fails to disclose the following:

a) dielectric layer is phosphosilicate glass.

However, Hess discloses a semiconductor device with a dielectric layer of phosphosilicate glass (For Example: See Column 4 Lines 56-59). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a dielectric layer of phosphosilicate glass as disclosed in Hess to aid in inhibiting the formation of phosphoric acid (For Example: See Column 4 Lines 29-42).

Additionally, since Hess and Hess are both from the same field of endeavor, the purpose disclosed by Hess would have been recognized in the pertinent art of Hess.

6. Claims 4, 14 and 26 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Burke et al. (U.S. Patent No. 6,102,528), Matta (U.S. Patent No. 6,183,067) and Hawkins (U.S. Patent No. 4,951,063).

In regards to claims 4 and 14, Hess fails to disclose the following:

a) the dielectric layer is comprised of a layer of thermal oxide and a layer of phosphosilicate glass.

However, Hawkins et al. ("Hawkins") discloses a dielectric layer with a layer of thermal oxide and a layer of phosphosilicate glass (For Example: See Column 4 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a dielectric layer with a layer of thermal oxide and a layer of phosphosilicate glass as disclosed in Hawkins to aid in protecting and insulating the heating elements (For Example: See Column 4 Lines 52-55).

Additionally, since Hess and Hawkins are both from the same field of endeavor, the purpose disclosed by Hawkins would have been recognized in the pertinent art of Hess.

In regards to claim 26, Hess fails to disclose the following:

a) the dielectric layer comprises of a layer of thermal oxide.

However, Hawkins discloses a dielectric layer with a layer of thermal oxide (For Example: See Column 4 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a dielectric layer with a layer of thermal oxide as disclosed in Hawkins to aid in protecting and insulating the heating elements (For Example: See Column 4 Lines 52-55).

Additionally, since Hess and Hawkins are both from the same field of endeavor, the purpose disclosed by Hawkins would have been recognized in the pertinent art of Hess.

7. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as obvious over Hess et al. (U.S. Patent No. 5,122,812) in view of Burke et al. (U.S. Patent No. 6,102,528), Matta (U.S. Patent No. 6,183,067) and Burke et al. (U.S. Patent No. 5,639,386).

In regards to claims 10 and 20, Hess fails to disclose the following:

a) transport mechanism for moving the fluid cartridge in at least one direction with respect to a recording media.

However, Burke et al. ("Burke") discloses a transport mechanism (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hess to include a transport mechanism as disclosed in Burke to aid in transporting the cartridge (For Example: See Figure 4).

Additionally, since Hess and Burke are both from the same field of endeavor, the purpose disclosed by Burke would have been recognized in the pertinent art of Hess.

Conclusion

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Ronen (U.S. Patent No. 4,288,801) discloses a switch array; b) Ronen (U.S. Patent No. 4,290,077) discloses a high voltage MOSFET; and c) Ronen (U.S. Patent No. 4,290,078) discloses a high voltage MOSFET.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
September 17, 2003

AMIR ZARABIAN
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